REMARKS

Claim 1 was objected to because of informalities. Claim 1 was amended to overcome the informalities.

Claims 1-3, 9, 10, and 12 stand rejected under 35 U.S.C. 102(e) as being anticipated by Dawson; claim 11 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Dawson in view of Wang.

Independent claim 1 includes the limitation of forming initial sidewall structures of similar widths. The Dawson et al. patent (US 5,963,803) describes forming sidewall structures of different widths 144 and 146 by first forming gate electrodes 122 and 126 of different heights. A single etch sidewall formation process is then used to form the sidewall structures 144 and 146 of different widths (col. 6, lines 51 to 58 clearly describe a single step process). Independent claim 1 of the instant invention describes a process which includes first forming sidewall structures of a first width using a first etching process. One set of the sidewall structures is then etched again to form sidewall structures of differing widths. This is not described nor taught in the Dawson et al. patent and therefore claim 1 is allowable over the cited art. In addition claims 2 and 3 depend form claim 1 and are also allowable over the cited art.

Independent claim also contains the limitation of first forming sidewall structures of a similar or first width and then selectively etching a set of the sidewalls to form sidewall structures of a differing width. As described above this feature is not found in the Dawson et al patent and claim 9 is allowable over the Dawson et al. patent. Claims 10 – 12 depend from claim 9 and are also allowable over the Dawson et al. patent. With regards to claim 10 the above-described feature is not taught nor described in the Wang et al. patent (US 6,020,231) and claim 10 is allowable over the Dawson et al. patent in combination with the Wang et al. patent.

In light of the above, it is respectfully submitted that the present application is in condition for allowance, and notice to that effect is respectfully requested.

While it is believed that the instant response places the application in condition for allowance, should the Examiner have any further comments or suggestions, it is respectfully requested that the Examiner contact the undersigned in order to expeditiously resolve any outstanding issues.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned **"Version with Markings to Show Changes Made."**

To the extent necessary, Applicants petition for an Extension of Time under 37 CFR 1.136. Please charge any fees in connection with the filing of this paper, including extension of time fees, to the deposit account of Texas Instruments Incorporated, Account No. 20-0668.

Respectfully submitted,

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Version with Markings to Show Changes Made

1. (Three Times Amended) A method of forming a CMOS sidewall spacer, comprising the steps of:

forming a PMOS transistor gate structure on a n-type region of a semiconductor substrate;

forming a NMOS transistor gate structure on a p-type region of said semiconductor substrate;

forming initial single layer sidewall structures of similar widths adjacent to said NMOS transistor gate structure and said PMOS transistor gate structure; and

etching said initial single layer sidewall structure adjacent to said NMOS transistor gate structure such that the width of the single layer sidewall structure adjacent to said NMOS transistor gate structure is less than the width of the single layer sidewall structure adjacent to said PMOS transistor gate structure.